Remarks

The present amendment is intended to be fully responsive to all points of rejection raised by the Examiner in the parent application and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1, 4 and 5 are pending in the application. Claims 1, 4 and 5 have been rejected. Claims 1, 4 and 5 have been amended.

New claims 7 - 13 have been added in order to more particularly point out what Applicant considers to be the invention. Applicant respectfully asserts that these claims are new and non-obvious and that no new matter has been added.

Double Patenting Rejections

In the Office Action, the Examiner rejected claims 1, 4 and 5 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 3 of US 6,297,096, the parent application to this one.

Enclosed herein is a terminal disclaimer.

Claim Rejections

35 U.S.C. § 102 Rejections

Claims 1, 4 and 5 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Hayabuchi - US 5,324,675) or, alternatively, under 35 U.S.C. § 102 (e) as being anticipated by Chang - US 5,836,772. Applicants respectfully traverse these rejections in view of the remarks that follow.

Hayabuchi discloses:

"Next, the silicon nitride layer 4 is subjected to thermal oxidation or CVD to form a second oxide layer 5 having a thichkness of approximately 40 Angstroms" (Col. 3, lines 66 – 68)

Hayabuchi clearly teaches away from "oxidizing a top oxide layer, thereby causing oxygen to be introduced into generally all of said nitride layer within said memory cell." (claim 1, lines 5 – 6), as recited in amended independent claim 1, since Hayabuchi will use either thremal oxidation or CVD deposition. In the latter (CVD), no oxidation of the nitride will occur. Moreover, Hayabuchi says

"Here, the thickness of the silicon nitride layer 4 is determined such that it can be entirely oxidized in a post-process described below, in which the silicon nitride layer 4 is oxidized except for the region thereof corresponding to the gate electrode described below " (col. 3, lines 61 – 65).

Hayabuchi's invention is that the nitride layer outside of the gate electrode region is fully oxidized. This is not "within said memory cell." Therefore, Hayabuchi cannot anticipate claim 1.

Similar arguments hold for amended claims 4 and 5. Hayabuchi does not introduce oxygen into the nitride of the cell; moreover, he teaches away from such. Therefore, Hayabuchi cannot anticipate claims 4 and 5.

Chang et al. discloses:

"Pinholes in the silicon nitride layer are preferably plugged with oxygen, most preferably by thermal treatment prior to formation of the top layer of silicon dioxide on the nitride layer". (Col. 2, lines 62 – 65)

Chang et al. does not teach or suggest "oxidizing a top oxide layer, thereby causing oxygen to be introduced into generally all of said nitride layer within said memory cell." (claim 1, lines 5 – 6), as recited in amended independent claim 1, since Chang et al. only teach to fill the pinholes during a process between formation of the nitride layer and that of the top silicon dioxide layer. Therefore, Chang et al. cannot anticipate claim 1.

Similar arguments hold for amended claims 4 and 5. In addition, it is noted that Chang et al. disclose:

"The present invention relates to a dielectric insulating composite for insulating a floating gate from a control gate in a nonvolatile memory cell such as EPROM, EEPROM and flash EPROM cells. The dielectric insulating composite includes a bottom layer of silicon dioxide formed on the floating gate, a layer of silicon nitride formed on the bottom silicon dioxide layer and a top silicon dioxide layer formed on the nitride layer where the silicon nitride layer has a thickness in the resulting composite which is less than the bottom and top silicon dioxide layers." (col. 2, lines 45 – 54)

Chang et al. does not teach or suggest "improving the charge retention in a nitride layer" as recited in amended independent claims 4 and 5 since the ONO layer of Chang et al. is used as a dielectric rather than as a charge retention layer. Therefore, Chang et al. cannot anticipate claims 4 and 5, as amended.

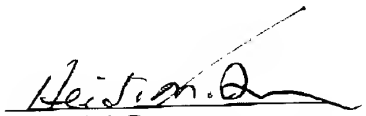
Accordingly, Applicant respectfully asserts that claims 1, 4 and 5 are allowable. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 1, 4 and 5.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit Account No. 05-0649.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Kindly amend claims 1, 4 and 5 as follows:

1. A method of fabricating an oxide-nitride-oxide (ONO) layer in a memory cell, said method comprising [the steps of]:

forming a bottom oxide layer on a substrate;

depositing a nitride layer; and

oxidizing a top oxide layer, thereby causing oxygen to be introduced into generally all of said nitride layer within said memory cell.

4. A method for improving the charge retention in a nitride layer of a memory [chip] cell, said method comprising [the steps of]:

depositing a nitride layer; and

introducing oxygen into generally all of said nitride layer within said memory cell.

5. A method for improving the charge retention in a nitride layer of a memory [chip] cell, said method comprising [the steps of]:

depositing a nitride layer;

controlling the thickness of said deposited nitride layer; and

introducing oxygen into generally all of said nitride layer within said memory cell.